EENG 284

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Digital Design Lab

Lab 2

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Hexadecimal to 7-segment converter

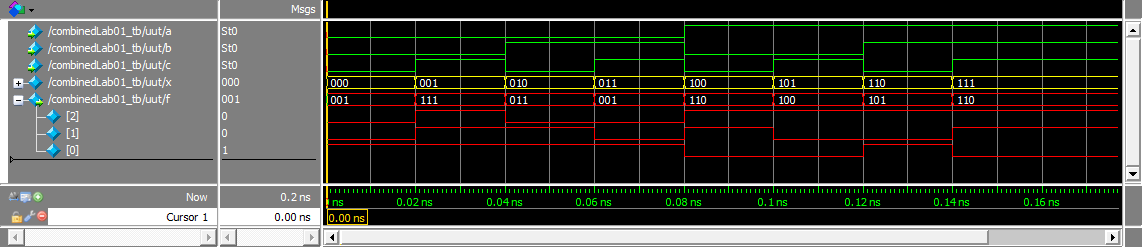
Lab Solutions

**Part 1:**

Truth Table for combinedLab01 function.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| a | b | c | f04 | f03 | f02 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

Timing diagram for combinedLab01 function



Pin assignment for combinedLab01

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Port | a | b | c | f[2] | f[1] | f[0] |
| Signal name | SW[2] | SW[1] | SW[0] | LEDR[2] | LEDR[1] | LEDR[0] |
| FPGA Pin No. | PIN\_AD13 | PIN\_AE10 | PIN\_AC9 | PIN\_G6 | PIN\_F6 | PIN\_F7 |

**Part 2:**

Truth Table for hexToSevenSeg function

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| x | seg[6] | seg[5] | seg[4] | seg[3] | seg[2] | seg[1] | seg[0] |
| 0000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0001 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0010 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0011 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0100 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0101 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0110 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0111 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1001 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1010 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1011 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1100 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1101 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1110 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1111 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

Verilog code for hexToSevenSeg function – just the always/case statement

always @(x)

case (x)

4'b0000: sevenSeg = 7'b1000000;

4'b0001: sevenSeg = 7'b1111001;

4'b0010: sevenSeg = 7'b0100100;

4'b0011: sevenSeg = 7'b0110000;

4'b0100: sevenSeg = 7'b0011001;

4'b0101: sevenSeg = 7'b0010010;

4'b0110: sevenSeg = 7'b0000010;

4'b0111: sevenSeg = 7'b1111000;

4'b1000: sevenSeg = 7'b0000000;

4'b1001: sevenSeg = 7'b0011000;

4'b1010: sevenSeg = 7'b0001000;

4'b1011: sevenSeg = 7'b0000011;

4'b1100: sevenSeg = 7'b1000110;

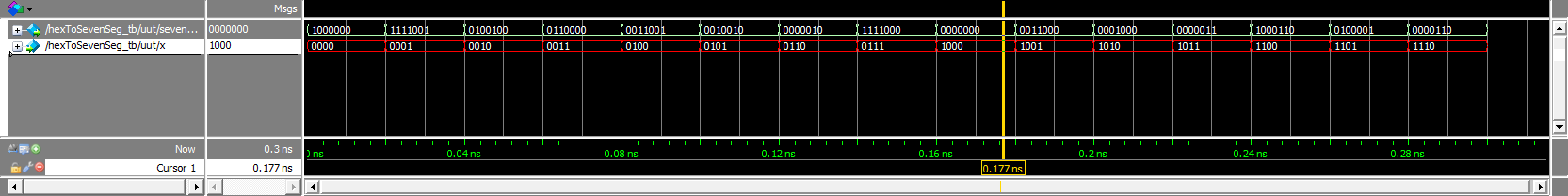
4'b1101: sevenSeg = 7'b0100001;

4'b1110: sevenSeg = 7'b0000110;

4'b1111: sevenSeg = 7'b0001110;

endcase

Timing diagram for hexToSevenSeg function



Pin assignment for hexToSevenSeg

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Port | x[3] | x[2] | x[1] | x[0] |
| Signal name | SW[3] | SW[2] | SW[1] | SW[0] |
| FPGA Pin No. | PIN\_AC8 | PIN\_AD13 | PIN\_AE10 | PIN\_AC9 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Port | sevenSeg[6] | sevenSeg[5] | sevenSeg[4] | sevenSeg[3] | sevenSeg[2] | sevenSeg[1] | sevenSeg[0] |
| Signal name | HEX0[6] | HEX0[5] | HEX0[4] | HEX0[3] | HEX0[2] | HEX0[1] | HEX0[0] |
| FPGA Pin No. | PIN\_Y18 | PIN\_Y19 | PIN\_Y20 | PIN\_W18 | PIN\_V17 | PIN\_V18 | PIN\_V19 |